Performance Analysis of High Frequency BJT and LDMOS Current Mode Class-D Power Amplifier

Mohammed Jashim Uddin, Syed Zahidur Rashid

Abstract— This work presents the design of a current mode class-D (CMCD) amplifier using simulation. Two separate designs are considered for simulation by using LDMOS FET and BJT with frequency range 1GHz to 3GHz. The CMCD architecture is an improvement over the Voltage Mode Class-D (VMCD) in that the parasitic reactance in the active device can be absorbed into the tank circuit resulting in a zero voltage switching condition. This amplifier has achieved a PAE of 54.08% with an output power of 39.29dBm (8.5W) and a gain of 9.94 dB at 2.6GHz with BJT. The simulation result of BJT shows high efficiency and higher bandwidth than LDMOS FET.

Index Terms— Biasing network, Current mode class D, LC tank, Q-factor, Radio frequency coil, Switching mode Power amplifier, Voltage mode Class D, Zero voltage switching and Zero current switching.

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1 INTRODUCTION

AMPLIFICATION is one of the most common and basic parameters in modern communication system. Power amplifier efficiency is a significant factor for the efficiency of most wireless systems. Poor efficiency of the power amplifier stage leads to large energy loss. It is not only deteriorating system efficiency, but also exacerbating thermal issues with devices "[1], [3]". The fast growth of wireless communication industries has created huge interest in the design of highly efficient, reliable and low-cost power amplifier. As the demand of video and data transmission increased in modern mobile communication system it will require continued development and improvement in the RF and microwave technologies [4]. Power amplifiers may be characterized by their efficiency, RF output power, linearity, mid-band frequency, relative bandwidth, gain, supply voltage and package size. There are various kinds of amplifier configurations that can maintain the above criteria such as class A, B, AB, C, D, E, F, inverse F and push-pull class B etc. Class D and class E are the most popular amplifiers. The class D amplifiers are widely used in power converter and low audio frequencies, but it is very little used in RF and microwaves frequencies [5]. In the recent years current mode class D (CMCD) switching mode amplifier topology has become the focus of the research to overcome the demands of high efficiency. CMCD amplifiers are reported using different device technologies, like GaAs FET [4], LDMOS [5] and GaN HEMTs [6], [7]. However, because the device acts as a switch, switching mode power amplifiers deliver a high efficiency, but are highly nonlinear. The practical limitations for reaching

100 %efficiency of RF and microwaves power amplifiers transistors are not ideal switches, because of parasitic reactances, finite on-resistance, limited gain and the load coupling network. Moreover, the different switching-mode power amplifier (SMPA) classes, class E, inverse F and current-mode class D (CMCD) have the advantage of providing zero voltage switching (ZVS). During the transition time of transistors from the OFF- to the ON-state the voltage across the output terminal of the device is zero [8], [9]. However, due to the parasitic reactive elements and high on-resistance of the power devices, class-D and E amplifier shows limited efficiency in terms of achievable frequency and power [10]. Actually, it is difficult to maintain the high efficiency at RF and microwaves frequencies because the output shunt capacitance of the transistors causes significant loss "[10], [12]".The class-E amplifier topology solves this problem by achieving zero voltage switching (ZVS) operation [5]. However, uncertain duty cycle, nonlinear capacitance, and other parasitic reactances can degrade class-E operation [13].For the last few years SMPA has been implemented with different technologies and different output power capabilities. Nevertheless, some published works are implemented and shows different performances; e.g.; a CMCD power amplifier for the base-station applications has also shown to achieve 60% drain efficiency with high output power which is 13W [5]and another CMCD amplifiers with 76.3% power-added efficiency (PAE) at 290mW output operating at 900MHz [4]. An amplifier from a closely related class-E/F with 85% drain efficiency at 7MHz has also been reported [14]. Also, a frequency operation of 700MHz achieved an output power of 0.89W with 78.5% collector efficiency [15]. In this paper performance analysis of LDMOS and BJT current mode class-D power amplifier is done with operating frequency 1GHz to 3GHz.

2 BASIC CONCEPT OF CMCD AMPLIFIER

2.1 CMCD Switching

Traditionally, the class-D PA circuits are the transformer coupled current-mode class-D (CMCD) PA and the transformer-

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coupled voltage mode class-D (VMCD) PA as shown in figure 1 and figure 2 respectively. The CMCD topology consists of two transistors, an LC parallel resonant circuit at the fundamental frequency and RF chokes (RFC). The difference between the CMCD PA and the VMCD PA is the biasing of the output-transformer centre tap and the LC tank configuration [2].If the LC resonator is connected in series to the load and the bias is supplied via a constant voltage, the configuration operates in voltage mode. If the tank is connected to ground or placed between the outputs of the two devices and the bias is a constant current, the circuit will operate in current mode. The input drive for the two transistors (TI, T2) should be of equal amplitude with 180^0 phase difference. This inversion is performed by the input balun transformer and another balun is also used at the output to provide the balanced load. In case of CMCD, current sources are used instead of voltage sources, and the two switching transistors control the current instead of the voltage [2]. By driving two transistors 180^0 out-of-phase, the current through the transistors is a square wave, while the voltage across the transistors is a half sine wave. The LC resonator provides a short circuit for higher order harmonics and only the fundamental component can reach to the load.
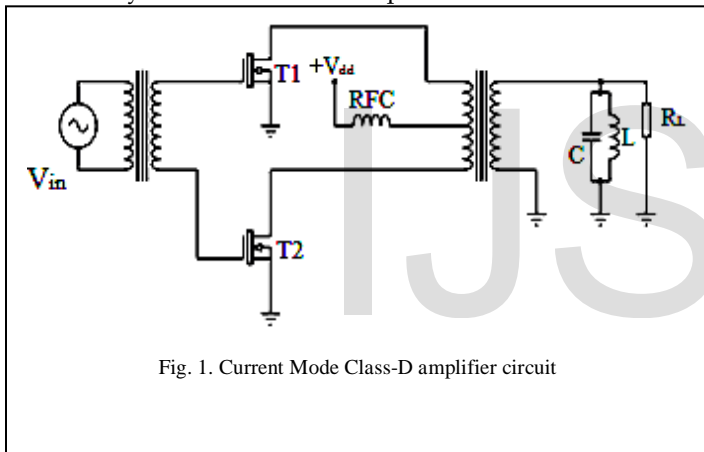

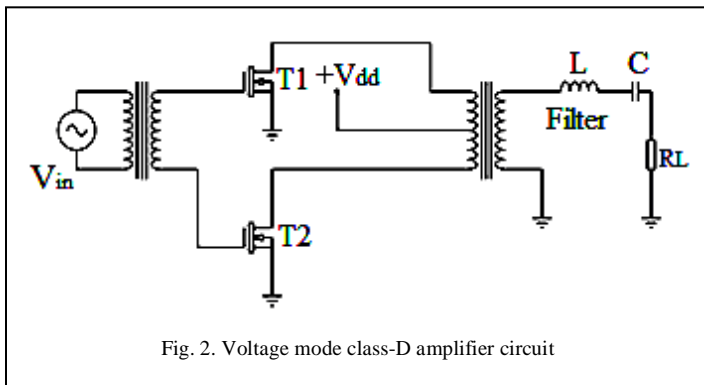Fig. 1. Current Mode Class-D amplifier circuit

Fig. 2. Voltage mode class-D amplifier circuit

Due to the filter resonance, there is no voltage across the transistors at each switching time and so-called zero voltage switching (ZVS) is achieved. This means that the output capacitance discharge problem is eliminated. Even if the transistors have some output capacitance, the output capacitance can become part of the output parallel filter. This ZVS feature is a key advantage of the CMCD architecture [4]. Another important switching condition, zero-current- switching (ZCS),

can avoid inductive losses by making the current zero at the instant of switching. But ZCS is less important than ZVS. Therefore, to form the voltage and current waveforms for CMCD, the harmonics of the tank resonant frequency must be treated appropriately. In this paper ZVS is considered for performance analysis.

3 SYSTEM ANALYSIS OF CMCD

In CMCD theoretical efficiency is 100% because of the non-overlapping voltage and current waveforms. In practice, at higher frequencies efficiency is limited, because of the parasitic reactive elements, device on-resistance, and difficulty in achieving low loss harmonic termination circuitry. It is much more difficult to obtain ideal voltage and current waveforms. Generally, the parasitic parallel capacitance C_{ds} across the drain-source terminals is quite more important than the parasitic series inductance L_{series} at the drain terminal [4]. This leads to energy dissipation through inductance and capacitance whenever the switch is closed. To minimize this energy dissipation, ideally V_{DS} must be zero which is called ZVS. The transistors T1 and T2 in CMCD amplifier circuit can be represented as a single switch model by considering parasitic inductance and capacitance effect at two different conditions. These switching models are shown in figure 3(a) and 3(b) for two kinds of consequences.
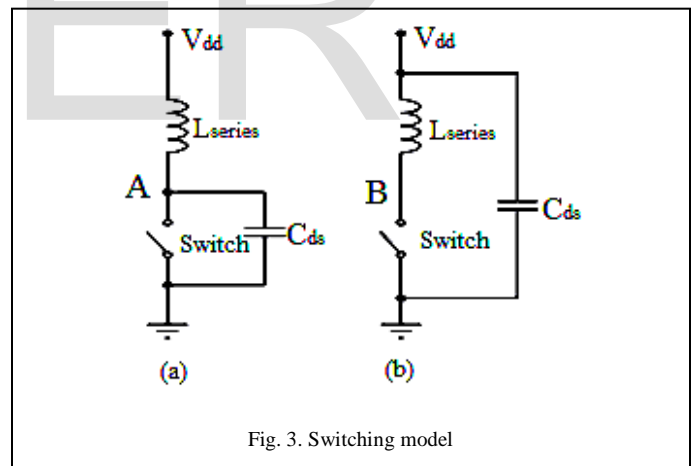

Fig. 3. Switching model

3.1 Input Current

In an ideal condition, the drain–source voltage V_{DS1}, V_{DS2} are half-rectified sine waves and the drain currents I_{DS1}, I_{DS2} are square waves. If the voltage source is V_{DD} then peak drain voltage can be calculated by

$$\int_0^T V_{DS}(t).dt = TV_{dd} \tag{1}$$

$$\text{And,} \int_0^{\frac{T}{2}} V_{peak}.\sin(wt).dt = 2V_{peak} \tag{2}$$

By combining equation (1) and (2) where put T=2π can be obtained

$$V_{peak} = \pi . V_{dd} \tag{3}$$

Let us assume that the transformer ratio, $n : m$ is 2: 1 in Fig. 1
So, output power can be calculated by

$$P_{out} = \frac{1}{2} \frac{(V_{peak})^2}{R_{load}} = \frac{1}{2} \frac{(\pi . V_{dd})^2}{R_{load}} = \frac{\pi^2}{2} \frac{V_{dd}^2}{R_{load}} \tag{4}$$

In an ideal situation, $P_{out} = P_{in}$ thus, the dc drain current can be expressed as

$$P_{out} = V_{dd} . I_{dc} \tag{5}$$

Or, $I_{dc} = \dfrac{P_{out}}{V_{dd}} = \dfrac{\pi^2}{2} \dfrac{V_{dd}}{R_{load}}$ (6)

3.2 Harmonic Components

A Fourier-analysis of the I_{DS} square wave reveals that it only contains odd harmonics and for the V_{DS} half sine shows that this waveform only contains even harmonics. High–order harmonic frequencies are needed for perfect half-rectified sine or square waves. In this calculation, parallel tank filter and balanced circuits considered as ideal. Therefore, ignoring harmonic components of V_{DS} and I_{DS} greater than third order voltage and current equation can be described as

$$V_{DS}(t) = V_{dd} + V_1 \sin(wt) - V_2 \cos(2wt) \tag{7}$$

$$I_{DS}(t) = I_{dc} - I_1 \sin(wt) - I_3 \sin(3wt) \tag{8}$$

Then the coefficient for the above equations can be calculated by applying following condition which are

$$\frac{d^2 V_{DS}}{d^2 t}\Big|_{wt=\frac{3\pi}{2}} = 0 \quad \text{And,} \quad \frac{d^2 I_{DS}}{d^2 t}\Big|_{wt=\frac{\pi}{2}, \frac{3\pi}{2}} = 0 \tag{9}$$

By second order derivation of equation (7) and (8), we can determine V_1, V_2, I_1, I_2

$$V_1 = \frac{4}{3} V_{dd} \tag{10}$$

$$V_2 = \frac{1}{3} V_{dd} \tag{11}$$

$$I_1 = \frac{9}{8} I_{dc} \tag{12}$$

$$I_2 = \frac{1}{8} I_{dc} \tag{13}$$

By substituting the above coefficients into the drain to source voltage and current equations, the following equations can be obtained.

$$V_{DS1} = V_{dd} + \frac{4}{3} V_{dd} \sin(wt) - \frac{1}{3} V_{dd} \cos(2wt) \tag{14}$$

$$I_{DS1} = I_{dc} - \frac{9}{8} I_{dc} \sin(wt) - \frac{1}{8} I_{dc} \sin(3wt) \tag{15}$$

$$V_{DS2} = V_{dd} - \frac{4}{3} V_{dd} \sin(wt) - \frac{1}{3} V_{dd} \cos(2wt) \tag{16}$$

$$I_{DS2} = I_{dc} + \frac{9}{8} I_{dc} \sin(wt) + \frac{1}{8} I_{dc} \sin(3wt) \tag{17}$$

For further analysis by considering up to fifth harmonics the above equations can be rewritten as follows:

$$V_{DS1} = V_{dd} + \frac{64}{45} V_{dd} \sin(wt) - \frac{4}{9} V_{dd} \cos(2wt) - \frac{1}{45} V_{dd} \cos(4wt) \tag{18}$$

$$I_{DS1} = I_{dc} - \frac{75}{64} I_{dc} \sin(wt) - \frac{25}{128} I_{dc} \sin(3wt) - \frac{3}{128} I_{dc} \sin(5wt) \tag{19}$$

3.3 Input and output power

The fundamental relationship between voltage and current can be expressed as for the transformer ratio, n : m is 2: 1 as

$$I_1 = \frac{2.V_1}{R_{load}} \tag{20}$$

Finally, with the help of above equations the total dc input current, dc input power and output power are described by

$$I_{dc-total} = I_{ds1} + I_{ds2} = 2.I_{dc} = \frac{16}{9} I_1 \tag{21}$$

$$P_{dc\_in} = I_{dc-total} . V_{dd} = \frac{16}{9} I_1 V_{dd} = \frac{128}{27} \frac{V_{dd}^2}{R_{load}} \tag{22}$$

$$P_{out} = \frac{1}{2} \frac{(2.V_1)^2}{R_{load}} = \frac{1}{2} \frac{(8/3.V_{dd})^2}{R_{load}} = \frac{32}{9} \frac{V_{dd}^2}{R_{load}} \tag{23}$$

3.4 LC tank design

The tank circuit is a combination of an inductor and capacitor with internal parasitic resistance. The parasitic resistance R_p limits the performance of the amplifier, as it contributes to the loss in the tank circuit. Moreover, the losses for package and lead parasitic and printed traces present inductance between the drain of the transistor and the tank, can also be prevented by perfect operation and tuning of the tank circuit. Modern chip inductors with series resistance less than 0.1 ohms and high quality ceramic chip capacitors with series resistance of 0.06 ohms or lower than that dominates the LC tank design for modern communication system [3].The following equations are mainly used to design the tank circuit's values of L and C. The angular frequency can be defined as

$$\omega = \omega_0 = 2\pi f \tag{24}$$

Quality factor Q is one of the essential parameter to sets the

bandwidth for operating frequency of an amplifier. A high Q will limit the operating bandwidth of the amplifier but will help to control the harmonics. So the bandwidth (BW) and quality factor Q can calculate by the following equations

$$BW = \frac{\omega_0}{Q} \tag{25}$$

And,

$$Q = \omega_0 C R_p \tag{26}$$

Here, R_p is the parasitic resistance of tank inductor and capacitor which can be written as

$$R_p = R_{Inductor} + R_{capacitor}$$

Having the suitable value for the Q it is easy to determine the inductor (L) and capacitor (C) as follows

$$C = \frac{Q R_p}{\omega} \tag{27}$$

$$L = \frac{1}{\omega^2 C} \tag{28}$$

4 DESIGN METHODOLOGY

In this paper basically a class-D power amplifier is proposed which is driven through current source. Thus it can be called current mode class-D PA. The schematic design is carried out with Harmonic-Balance simulator of Microwave Office AWR. The key advantage of using simulation approach is that it alleviates time consuming and potential difficult measurement which is involved expensive experimental setup. Input and output matching of switching device is done through lumped element provided by the software package. A design approach is also used for the LC resonator filter of current mode class-D power amplifier. The trial and error method is used for tuning tank circuit. The proposed design methodology is used to find the output power, gain, total power and PAE of design circuit. Finally, it is simulated through simulation software for a frequency range of (1-3) GHz.

4.1 Schematic design architecture

In this design a wideband balun is used for both BJT and LDMOS with a lumped element tank that provides proper harmonic impedances for maximum efficiency of the device. This balun has 180^0 phase shift between two ports at least
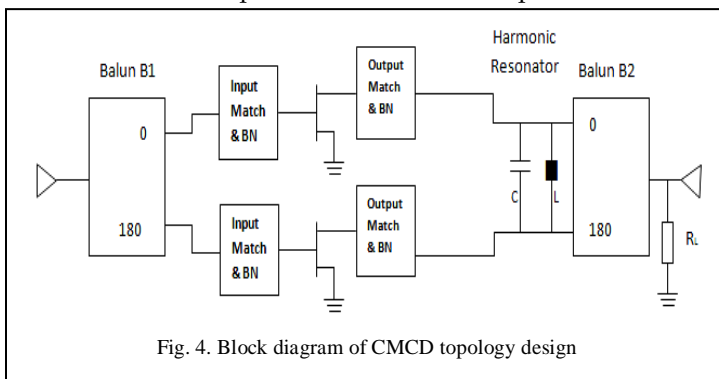

Fig. 4. Block diagram of CMCD topology design

up to the third harmonic. On the other hand different input and output matching network is introduced for both devices. The block diagram of the CMCD topology is used in this work for sweep frequency 2.6 GHz is shown in figure 4.

4.2 Device approach

High power RF transistors characterization is difficult without a clear understanding of the device. Some companies provide the design models of the transistor and some of them are published. In this project Motorola MRF19030 LDMOS FET and high power BJT MRA 0500-19L are chosen for designing current mode class-D power amplifier design. The datasheet of LDMOS is available but it is very difficult to find the datasheet for BJT. Both transistor models which are used for these simulations are collected from Microwave Office AWR System software package library. The maximum operating voltage for LDMOS FET is $V_{DS} = 32V$ with a corresponding on-state breakdown voltage of $BV_{DS} > 65V$. Some notable characteristics of this transistor are listed in Table 1. All measurements are done at a sweep frequency of 2.6GHz.

TABLE 1
LDMOS DEVICE PARAMETER

Parameters	Value
C_{ds}	6pF
Breakdown voltage	65V
Gate voltage	3V
Output power	4.5W
Power gain	13.5dB

5 SIMULATION RESULTS

In this work, two simulation setups, for both LDMOS and high power BJT switching device, are considered. One is for power gain and another one is for output power and PAE efficiency simulation. Also, the simulation for both LDMOS and BJT are performed at the same frequency range (1-3) GHz and 2.6 GHz sweep frequency, but different input power (for BJT 30dBm and for LDMOS 12.7dBm) is considered. Figure 5 shows the simulation result of the power gain for BJT and LDMOS FET. In the case of BJT the output power shows nearly flat response which means that current mode class-D power amplifier of BJT has wide operating bandwidth. On the other hand, the frequency response for LDMOS FET indicates that LDMOS current mode class-D power amplifier has low operating bandwidth rather than BJT which is used in this design. Figure 6 represents power added efficiency (PAE) performance of PA over frequency range 1GHz to 3GHz. The maximum PAE obtained for bipolar transistor is 17% with respect to 3GHz frequency. Alternatively, Lateral Double-Diffused Metal-Oxide-Semiconductor transistor gives very poor PAE. The lumped passive elements such as resistors, inductors and capacitors are applied for input and output matching which degrade efficiency.
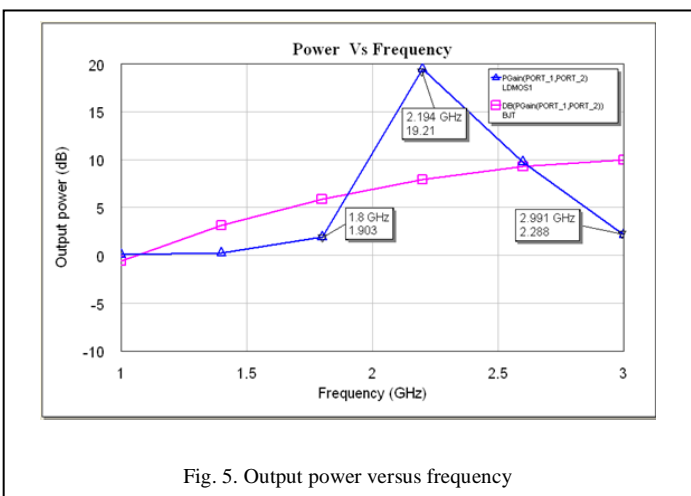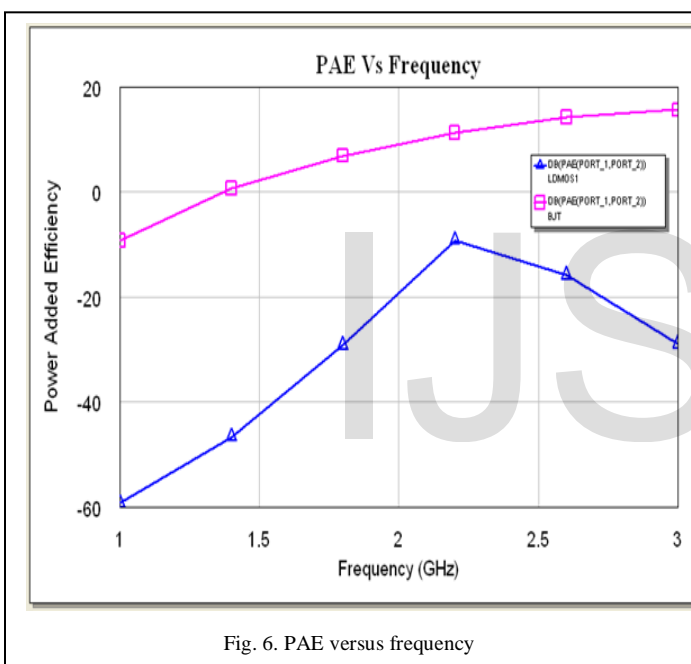
Fig. 5. Output power versus frequency
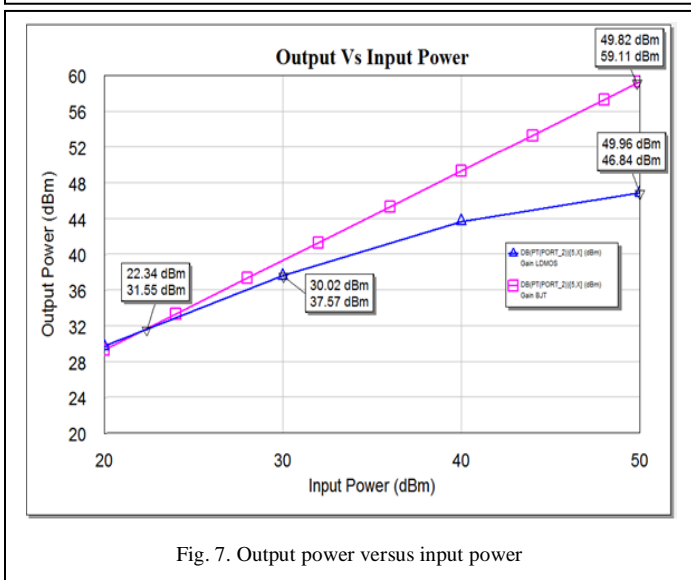

Fig. 6. PAE versus frequency

Fig. 7. Output power versus input power

Figure 7 shows the simulation result of output power current mode class-D power amplifier of BJT and LDMOS FET with respect to input power. The linear curve (pink) in the graph represents the output power of BJT and the curve below (blue) represents the output power of LDMOS. It is observed that BJT has linear output power throughout the total input power ranging from 20dBm to 50dBm. However, BJT CMCD comparatively has low output power than LDMOS before 22dBm input power. The 22.34dBm input power is the transition point for both amplifiers. It also shows that for the 30dBm input power the output power is 39.29dBm for BJT and 37.57dBm for LDMOS. But P_{out} of FET is decreasing after 50dBm input power. Table 2 shows the value of output power of both devices for several input power.

TABLE 2
OUTPUT POWER OF BJT AND LDMOS

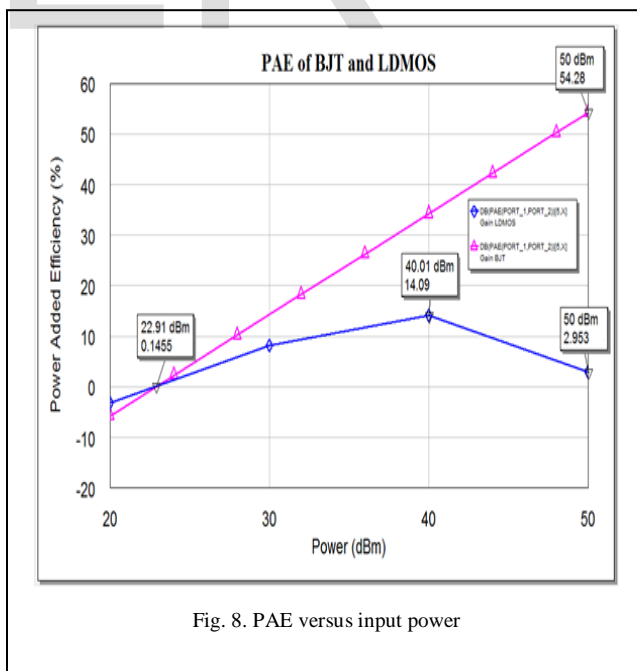| Input Power (dBm)	Output Power (dBm) of BJT	Output Power (dBm) of LDMOS
10	19.3	19.88
12.7	**22**	**23**
15	24.3	24.89
20	29.3	29.73
25	34.3	34.11
30	**39.29**	**37.56**
35	44.3	40.07
40	49.3	43.67
45	54.3	46
50	59.3	46.85
55	64.3	44.36

Fig. 8. PAE versus input power

Figure 8 exposes the result of power added efficiency of CMCD power amplifier for device used in this paper with respect to input power. The linear characteristics of bipolar transistor are remained same in the η_{PAE} graph whereas it is

slightly changed for LDMOS. The transition point of both amplifiers is improved by 1dBm in power added efficiency measurement as compared with input power. At that transition point both amplifiers show less than 1% efficiency which means that the minimum input power needed for both amplifier is almost 23dBm (200mW). The highest efficiency achieved for bipolar transistor is 54.28% at P_{in} =50dBm and 14.09% for LDMOS transistor at P_{in} = 40dBm. The η_{PAE} of LDMOS greatly decreased from 40dBm to 50dBm and reached 2.93% efficiency at maximum input power. It indicates that BJT can handle large input and output power and LDMOS has limited input and output power capability. It is assumed that non-ideal RF chokes used in the drain as a current source can decrease the PAE of LDMOS. It is seen that the maximum PAE and P_{out} are reached at the maximum drive power. The output power and power-added efficiency (PAE) increased dramatically with increasing the input power in the case of BJT. The desired ZVS condition is not quite achieved for LDMOS FET and the efficiency is degraded. In addition, as the input power is increased, the transition point of both CMCD also increased. The minimum and maximum variation of output power for both designs is 0.85dBm and 12.45dBm. On the other hand, the variation of η_{PAE} is large enough for two CMCD at higher P_{in}. From figure 5, it can be seen that the differences of gain at 2.2 GHz is the largest which is nearly 11.61dB.

TABLE 3
COMPARISON TABLE OF PUBLISHED CMCD WITH THIS WORK

Ref.		f (GHz)	P_{out} (dBm)	G (dB)	PAE (%)
[1]		1.8	47	10	56.7
[15]		0.7	29.5	9	68.5
[4]		0.9	24.6	12	76.3
[5]		1.0	41.1	14	58
[6]		1.0	38.5	9.5	55.8
[7]		1.0	43.1	15.1	68.8
This Work	BJT	2.6	**39.29**	9.94	**54.08**
	LDMOS	2.6	23	19.21	14.09

One of the reasons may be the consideration of only up to third harmonic termination. Moreover, second and third harmonic termination is not perfect due to parasitic element of the devices. The overall comparison of this work with previous work is listed in the Table 3.

6 CONCLUSION

In this paper high power current mode class-D amplifier using LDMOS FET and BJT is designed and simulated for RF and microwave frequency application. The completed amplifier achieved a PAE of 54.08% for an output power of 39.29dBm

(8.5W) and a gain of 9.94 dB at 2.6GHz with BJT. The operating frequency of this PA is the highest compared to other published CMCDs. The simulation result of BJT confirmed that high efficiency can be obtained and shows the possibility of higher bandwidth limitation. The presented result proves that usage of lumped element in input and output matching can achieve high output power and power added efficiency. Due to the linear characteristics of output power, this type of amplifier is suitable for wireless system applications in both polar and envelope based modulation.

7 FUTURE WORKS

In this work only up to third harmonics is considered, so a closer investigation of higher order harmonics treatment is necessary. Additionally, it would be interesting to investigate and characterize the tank circuit resonator quality factor (Q). It is believed that decreasing the resonator Q will improve the performance. The quality factor of tank circuit is inversely proportional to the frequency which means lower value of Q will offer high frequency. However, the inductance is very much sensitive with high frequency which should be used in CMCD PA design. So it will have a great impact for the researchers in near future.

8 ACKNOWLEDGMENT

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